

PRE-PATTERN SURFACE MODIFICATION FOR LOW-K DIELECTRICS

FIELD OF THE INVENTION

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The invention is generally related to the field of forming interconnect layers in a semiconductor device and more specifically to patterning low-k dielectric films.

BACKGROUND OF THE INVENTION

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As the density of semiconductor devices increases, the resistance-capacitance (RC) delay time in the back-end-of the-line (BEOL) increases and dominates the circuit performance. To reduce RC delay time at BEOL, the demands on interconnect layers for connecting the semiconductor devices to each other also increase. Therefore, there is a desire to switch from the traditional aluminum metal interconnects to copper interconnects and from traditional silicon-dioxide-based dielectrics to low-k dielectrics, such as organo-silicate glass (OSG). Semiconductor fabrication processes for working with the copper interconnects and newer low-k dielectrics are still needed.

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As compared to the traditional subtractive plasma dry etching of aluminum, suitable copper etches for a semiconductor fabrication environment are not readily available. To overcome the copper etch problem, damascene processes have been developed. In a damascene process, the IMD (intra-metal dielectric) is formed first. The IMD is then patterned and etched to form trenches for the interconnect lines. If connection vias have not already been formed, a dual damascene process may be used. In a dual damascene process, an ILD (interlevel dielectric) is deposited before the IMD. An etch-stop layer, such as SiN, can be optionally used in between the IMD and the ILD. The via is formed in the ILD for connection to lower interconnect levels and the trench is formed in the IMD. A barrier layer and a copper

seed layer are then deposited over the structure. The barrier layer is typically tantalum nitride or some other binary transition metal nitride. The copper layer is electrochemically deposited (ECD) using the seed layer over the entire structure. The copper is then chemically-mechanically polished (CMP'd) to remove the copper from over the IMD, leaving copper interconnect lines and vias. A metal etch is thereby avoided.

When low-k dielectrics such as OSG are used for the IMD and ILD, a problem known as resist poisoning occurs. Resist poisoning occurs during a patterning step such as via pattern or trench pattern. It is a result of the interaction between a DUV (deep ultra-violet) resist and low-k films. Resist poisoning causes poor resist sidewall profiles, resist scumming, and large CD variations. Furthermore, the required resist exposure dose to achieve the target CD becomes too high and varies with film aging. A process to reduce or eliminate resist poisoning in low-k dielectrics is therefore desired.

SUMMARY OF THE INVENTION

The invention is a surface treatment for low-k films that improves patterning. The low-k film is treated with a dry-wet (D-W) process to eliminate or significantly reduce resist poisoning. An optional dry (D) process can follow the D-W process. The D-W or D-W-D treatment can be performed at various stages in the semiconductor fabrication process with or without the presence of resist. For example, this treatment can be applied to as-deposited low k films before patterning (pre-treatment) or to stripping photoresist for lithograph rework.

An advantage of the invention is providing a treatment to reduce or eliminate resist poisoning of low-k dielectric films.

This and other advantages will be apparent to those of ordinary skill in the art having reference to the specification in conjunction with the drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

- 10 FIGs. 1A-1F are cross-sectional diagrams of a process for forming metal interconnects according to the embodiments of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The invention will now be described in conjunction with dual damascene copper interconnect process. It will be apparent to those of ordinary skill in the art that the benefits of the invention may be applied generally to patterning of low-k ($K < 3.0$) and ultra-low-k ($K < 2.5$) films.

In order to form the copper interconnects using a dual damascene process, the interlevel dielectric (ILD 102) and intrametal dielectric (IMD 104) in FIG. 1A are patterned and etched to form trenches in IMD 104 and vias in ILD 102. When low-k or ultra low-k materials are used for the ILD and IMD, an interaction between the resist and the low-k materials causes resist poisoning. The cause of resist poisoning is believed to be the interaction of between the DUV resist and nitrogen-containing reagents from the low-k films. Possible sources of nitrogen include: the low-k film, the dielectric cap, the optional IMD etch-stop layer (e.g., SiN), N_2 in the clean (ash) process, N_2 in the etch chemistry, and the photoresist itself.

In order to reduce or eliminate the resist poisoning, a pre-pattern treatment using a dry-wet (D-W) or dry-wet-dry (D-W-D) process is performed. The dry process comprises a reducing-type plasma with a gas chemistry of H_2 with an inert gas such as argon or nitrogen. The first dry process is an ash-type process. The wet process functions as a clean to remove any etch polymers and surface particles. The wet chemistry may comprise one of the following: HF/organic acid (such as citric, acetic, gallic, and oxallic); HF; citric; a solvent such as NE-14 (a solvent from Ashland) or AP360 (a solvent from ATMI); or H_2SO_4 . The final optional dry process is used for passivation and may also be comprised of H_2/N_2 or H_2/Ar plasma. In the preferred embodiment, a H_2/Ar plasma is used followed by treatment with the NE-14 solvent from Ashland.

As an example, the following H₂/Ar plasma process may be used for the first dry step:

Time: 1-3 min., preferably 2 min.
Pressure: 500-1500 mT, preferably 700 mT
5 Power: 600-1000 W, preferably 950 W
Flow: 1000-3000 sccm H₂, preferably 3000 sccm
500-2000 sccm Ar, preferably 2000 sccm
Chuck Temp.: 150-265 °C, preferably 250°C

10 For the wet step, the process conditions depend on the solution used. For example, for H₂SO₄ a temperature in the range of 56-61°C is optimal. In addition, the surface of the structure may be pre-wet with a wetting agent such as deionized water. As another example, NE-14 may be used at a temperature in the range of 23°C to 35°C, preferably 27°C for a duration in the range of 5-20
15 minutes, preferably 5 minutes.

For the final dry step, the following H₂/Ar plasma process may be used:

Time: 1-3 min., preferably 2 min.
Pressure: 500-1500 mT, preferably 700 mT
20 Power: 500-1000 W, preferably 700 W
Flow: 300-1000 sccm H₂, preferably 500 sccm
300-1000 sccm Ar, preferably 500 sccm
Chuck Temp.: 50-75 °C, preferably 60°C

25 In both the initial and final dry steps, lower temperature and lower pressure give the best result at the cost of reduced rate (i.e., longer process time). Limitations of the current tool capabilities are also considered.

Embodiments of the invention will now be discussed with reference to
30 FIGs. 1A-1F. A semiconductor body 100 is processed through formation of the

ILD 102/IMD 104. Semiconductor body 100 typically comprises a silicon substrate having transistors and other elements formed therein. IMD 104 is the dielectric for a copper interconnect level. Copper interconnect level may be the first or any subsequent metal interconnect level of the semiconductor device 120.

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An ILD 102 is formed over semiconductor body 100. IMD 104 is formed over ILD 102. A trench etch-stop layer (not shown) may optionally be placed between ILD 102 and IMD 104. ILD 102 and IMD 104 comprise low-k or ultra low-k dielectrics, such as organo-silicate glass (OSG). In the preferred embodiment, ILD 102 and IMD 104 comprise the same material. However, ILD 102 and IMD 104 may alternatively comprise different materials. A capping layer (not shown) may be formed over IMD 104 if desired. Typically, the capping layer comprises silicon nitride, Alternatively, silicon oxide, silicon oxynitride (SiON), or Si-rich nitride (SRN) or SiC capping layer, or no capping layer may be used.

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In a first embodiment of the invention, the pre-pattern D-W or D-W-D treatment is performed prior to forming the via pattern 130. Then, the via pattern 130 is formed as shown in FIG. 1B. The pre-pattern D-W or D-W-D treatment reduces resist poisoning at the via pattern level.

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It is sometimes necessary to rework a resist pattern. Rework is a process of removing the photoresist and/or BARC material for re-patterning. Pattern rework significantly worsens the resist poisoning problem if a non-optimized ash process is used for re-work. Accordingly, in a second embodiment of the invention, the D-W or D-W-D treatment is used to rework via pattern 130. Using the D-W or D-W-D treatment according to the invention as a pattern re-work reduces or eliminates resist poisoning associated with the via pattern.

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When the D-W or D-W-D treatment is instead used in addition to a

conventional wet or dry resist rework process, resist poisoning is caused by the other processing is only reduced. Accordingly, it is preferred to use the D-W or D-W-D process as the pattern re-work instead of in addition to other rework processes.

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After any desired pattern re-work, the via 106 is then etched through IMD 104 and ILD 102, as shown in FIG. 1C.

10 In order to protect the bottom of via 106 during the subsequent trench etch, via 106 may be partially or completely filled. For example, an organic barc (bottom anti-reflection coating) may be deposited over the structure and etched back such that BARC material remains only in the vias 106.

15 After a post via etch clean, the D-W or D-W-D process of the invention may be used as a pre-trench pattern treatment. For some applications, pre-treatment at the trench pattern level may be more critical than at the via pattern level.

20 After the post via clean and any desired pattern pre-treatment, a trench pattern 132 may be formed over IMD 104, as shown in FIG. 1D. After any desired pattern rework, a trench 108 is etched in IMD 104, as shown in FIG. 1E. Trench pattern 132 is then removed.

25 Barrier layer 110 is deposited over IMD 104 including in trench 108 and via 106. Barrier layer 110 functions to prevent copper diffusion into the ILD and IMD layers. Suitable barrier materials such as Ta/TaN are known in the art. A seed copper layer is then deposited over barrier layer 110.

30 Electrochemical deposition (ECD) may then be used to deposit copper layer 124. Various copper ECD processes are known in the art. In one example,

a 3-step process is used. After placing the wafer in the plating solution, a current of approximately 0.75 Amps is passed through the seed layer for a time on the order of 15 seconds. The current is then increased to around 3 Amps for approximately 60 seconds. Final plating occurs at a current of about 7.5Amps with the duration determined by the final desired thickness. A quick spin-rinse dry (SRD) is performed in the plating cell above the plating solution. The wafer is then transferred to the SRD cell and a post-ECD SRD is used to clean the plating residue.

After copper ECD, the copper 124 and barrier 110 are chemically mechanically polished (CMP) to remove the material from above IMD 104. The resulting structure is shown in FIG. 1F. Next level ILD and IMD may be deposited and processing may then continue to form additional metal interconnect levels and package the device.

As a result of the D-W or D-W-D treatment according to the invention, the DUV pattern energy required to achieve the target CD (critical dimension) is reduced, the via sidewall angle is increased and the depth of focus (DOF) is increased. In one set of experiments, the exposure energy was reduced to between 30 and 35 mJ/cm² for both types of photoresist tested. In the baseline approach without pre-pattern treatment, the exposure energies varied from 40-80mJ for one photoresist and 35-60 mJ for another photoresist. In the baseline approach, the via sidewall angle was typically less than 83° and a footing was present at the OSG surface. The via sidewall angle using the invention is increased to 85° and above. Moreover, the footing is eliminated. DOF between 0.4 μm and 6μm were achieved using the invention. Whereas, without pre-pattern treatment, the DOF varied from not being able to print at all (0) and 0.4 μm.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense.

Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the

5 art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.